



4/ 2177  
\$

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.      Art Unit: 2177  
Serial No.: 10/039,289      Examiner:  
Filed : January 4, 2002      Srirama Channavajjala  
Assignee : Intel Corporation  
Title : QUEUE ARRAYS IN NETWORK DEVICES

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RECEIVED

JUL 02 2004

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information  
Disclosure Statement and documents listed on form PTO-1449.

Kindly accept this Information Disclosure Statement under  
Rule 97(c)(2). The rule 17(p) certification fee of \$180 is  
enclosed.

The documents are in the English language; hence no concise  
explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the  
return of a copy of the enclosed form PTO-1449 with the

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

07/01/2004 ZJUHA1 00000135 10039289

01 FC:1806

180.00 OP

I hereby certify under 37 CFR §1.8(a) that this correspondence is being  
deposited with the United States Postal Service as first class mail with  
sufficient postage on the date indicated below and is addressed to the  
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

June 28, 2004  
Date of Deposit

Signature

Jennifer H. Payne

Typed or Printed Name of Person Signing Certificate

Applicant : Gilbert Wolrich et al.  
Serial No.: 10/039,289  
Filed : January 4, 2002

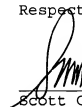
Attorney's Docket No.:10559-612001

Examiner's initials in the left column per MPEP 609 are  
earnestly solicited along with an early action on the merits.

Please apply any additional charges or credits to Deposit  
Account No. 06-1050.

Respectfully submitted,

Date: 6/28/04

  
\_\_\_\_\_  
Scott C. Harris  
Reg. No. 32,030  
Attorney for Intel Corporation

Fish & Richardson P.C.  
USPTO Customer No. 20985  
12390 El Camino Real  
San Diego, CA 92130  
Telephone: (858) 678-5070  
Facsimile: (858) 678-5099

10408056.doc


Sheet 1 of 2

Substitute Form PTO-1449

U.S. Department of Commerce  
Patent and Trademark Office

Attorney's Docket No.  
10559-612001

Application No.  
10/039,289

**Information Disclosure Statement  
by Applicant**

(Use several sheets if necessary)

(37 CFR §1.98(b))

Applicant  
Gilbert Wolrich et al.

Filing Date  
01/04/02

Group Art Unit  
2177

**RECEIVED**

JUL 02 2004

Technology Center 2100

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	09/475,614	12/1999	Wolrich, et al.			
	AB	09/473,571	12/1999	Wolrich, et al.			

**Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	✓ AC	WO 01/50679	07/2001	WIPO				
	✓ AD	WO 01/50247	07/2001	WIPO				
	✓ AE	WO 01/48619	07/2001	WIPO				
	✓ AF	WO 01/48606	07/2001	WIPO				
	✓ AG	WO 01/48596	07/2001	WIPO				
	✓ AH	WO 01/16782	03/2001	WIPO				
	✓ AI	WO 01/16770	03/2001	WIPO				
	✓ AJ	WO 01/16769	03/2001	WIPO				
	✓ AK	WO 01/15718	03/2001	WIPO				
	✓ AL	WO 97/38372	10/1997	WIPO				
	✓ AM	WO 94/15287	07/1994	WIPO				
	✓ AN	EP 0 809 180	11/1997	Europe				
	✓ AO	EP 0 745 933	12/1996	Europe				
	✓ AP	EP 0 633 678	01/1995	Europe				
	✓ AQ	EP 0 464 715	01/1992	Europe				
	✓ AR	EP 0 379 709	08/1990	Europe				
	✓ AS	59-111533	06/1984	Japan (w/abstract)				X

**Other Documents (include Author, Title, Date, and Place of Publication)**

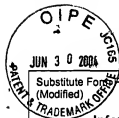
Examiner Initial	Desig. ID	Document
	AT ✓	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AU ✓	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 <sup>nd</sup> ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

Examiner Signature

Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)


Sheet 2 of 2
**RECEIVED**

JUL 02 2004

2177 Technology Center 2100

Substitute Form (Modified)	PTO-1449	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-612001	Application No. 10/039,899
<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)			Applicant Gilbert Wolrich et al.	
			Filing Date 01/04/02	Group Art Unit 2177

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AV	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	AX	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	AY	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	AZ	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225.
	AAA	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	ABB	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, <i>Online</i> , 13 November 1998.
	ACC	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	ADD	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28 <sup>th</sup> Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AEE	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines," pp. 22-28, 1998.
	AFF	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , pp. 1-20, 18 March 1999.
	AGG	Vibhatavanij et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-369.
	AHH	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

Substitute Disclosure Form (PTO-1449)